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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,594	04/15/2004	Fumitoshi Mizutani	ND-448US	6639

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EXAMINER	
TRUONG, LOAN	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,594	MIZUTANI ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Bartels et al. (2003/0208704).

In regard to claim 1, Bartels et al. disclosed an information processing apparatus, comprising:

first and second information processing means for performing the same process in synchronism with each other (*digital computing system with dual redundant lane system configure to take advantage of the redundant memory array arrangement and lane-to-lane cross compare feature lockstep architecture, fig. 1, 100, paragraph 0022)*; and

adjustment means for adjusting orders of output data from said first and second information processing means so as to correspond to each other to discriminate whether or not the output data coincide with each other (*error detection and correction components, fig. 1, 116, paragraph 0022).*

In regard to claim 2, Bartels et al. disclosed an information processing apparatus as claimed in claim 1, wherein said adjustment means includes first storage means for storing the output data of said first information processing means and second storage means for storing the output data of said second information processing means (*EDC component, fig. 1, 116, 118, 126, 128).*

In regard to claim 3, Bartels et al. disclosed an information processing apparatus as claimed in claim 2, wherein said adjustment means compares, when the amount of output data stored in any one of said first and second storage means reaches a predetermined amount (*dual redundant lane process in lockstep architecture, paragraph 0022)*, the output data of said first information processing means stored in said first storage means and the output data of said second information processing means stored in said second storage means with each other with the output data adjusted in order so as to correspond to each other to discriminate whether or not the output data coincide with each other (*write and read comparator, fig. 1, 114, 119, 124, 129, paragraph 0023 and paragraph 0026).*

In regard to claim 4, Bartels et al. disclosed an information processing apparatus as claimed in claim 2, wherein said adjustment means further includes designation means for designating the frequency with which the discrimination is to be performed to a frequency lower than a frequency with which the output data of said first and second information processing means are received (*generate an interrupt, fig. 2, paragraph 0030).*

The examiner interprets the lower in frequency implemented by the delay in clock cycle where a delay maybe established by an interrupt.

In regard to claim 5, Bartels et al. disclosed an information processing apparatus, comprising:

first and second information processing means for performing the same process in synchronism with each other (*digital computing system with dual redundant lane system configure to take advantage of the redundant memory array arrangement and lane-to-lane cross compare feature lockstep architecture, fig. 1, 100, paragraph 0022)*; and

adjustment means including re-construction means for re-constructing a plurality of output data of said second information processing means based on a plurality of output data of said first information processing means (*restore the fault-free copy to the faulted memory location, fig. 2, 240)*; and

comparison means for comparing the output data of said first information processing means and the output data of said second information processing means re-constructed by said re-construction means with each other (*perform bit-by bit comparison of first and second copies of data, fig. 2, 220, 245, paragraph 0030 and 0032).*

In regard to claim 6, Bartels et al. disclosed an information processing apparatus as claimed in claim 5, wherein said adjustment means includes first storage means for storing the output data of said first information processing means and second storage means for storing the output data of said second information processing means (*EDC component, fig. 1, 116, 118, 126,*

128), and said re-construction means changes the order of the output data of said second information processing means stored in said second storage means based on the order of the output data of said first information processing means stored in said first storage means (*restore the fault-free copy to the faulted memory location, fig. 2, 240).*

In regard to claim 7, Bartels et al. disclosed an information processing apparatus as claimed in claim 5, wherein said adjustment means includes first storage means for storing the output data of said first information processing means and second storage means for storing the output data of said second information processing means (*EDC component, fig. 1, 116, 118, 126, 128)*, and said re-construction means divides and re-couples (*EDC components utilize the error detection and correction linear block with the minimum properties of detecting and correcting all single bit faults within a data word, paragraph 0029)* the output data of said second information processing means stored in said second storage means based on the output data of said first information processing means stored in said first storage means (*restore the fault-free copy to the faulted memory location, fig. 2, 240).*

In regard to claim 8, Bartels et al. disclosed an information processing apparatus, comprising:

first and second information processing means for performing the same process in synchronism with each other (*digital computing system with dual redundant lane system configure to take advantage of the redundant memory array arrangement and lane-to-lane cross compare feature lockstep architecture, fig. 1, 100, paragraph 0022)*; and

adjustment means for selecting one of data of a second output of said second information processing means which corresponds to one of data of a first output of said first information processing means to detect whether or not the data of the first and second outputs coincide with each other (*write and read comparator, fig. 1, 114, 119, 124, 129, paragraph 0023 and paragraph 0026).*

In regard to claim 9, Bartels et al. disclosed an information processing apparatus as claimed in claim 8, wherein said adjustment means includes first storage means for storing the data of the first output of said first information processing means and second storage means for storing the data of the second output of said second information processing means (*EDC component, fig. 1, 116, 118, 126, 128)*, and said adjustment means searches said second storage means for one of the data of the second output corresponding to one of the data of the first output of said first information processing means stored in said first storage means (*restore the fault-free copy to the faulted memory location, fig. 2, 240).*

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Loan Truong
Patent Examiner
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SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER